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121 Tools and methods for the verification of processors and processor-based systems: IODINE: a tool to automatically infer dynamic invariants for hardware designs
Sudheendra Hangal, Naveen Chandra, Sridhar Narayanan, Sandeep Chakravorty
June 2005 **Proceedings of the 42nd annual conference on Design automation**
Publisher: ACM Press
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We describe IODINE, a tool to automatically extract likely design properties using dynamic analysis. A practical bottleneck in the formal verication of hardware designs is the need to manually specify design-specic properties. IODINE presents a way to automatically extract properties such as state machine protocols, request-acknowledge pairs, and mutual exclusion between signals from design simulations. We show that dynamic invariant detection for hardware designs can infer relevant and accurate ...

Keywords: dynamic analysis, dynamic invariants, formal specification

122 SAT: cool algorithms and hot applications: Efficient SAT solving: beyond supercubes
Domagoj Babić, Jesse Bingham, Alan J. Hu
June 2005 **Proceedings of the 42nd annual conference on Design automation**
Publisher: ACM Press
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SAT (Boolean satisfiability) has become the primary Boolean reasoning engine for many EDA applications, so the efficiency of SAT solving is of great practical importance. Recently, Goldberg *et al* introduced *supercubing*, a different approach to search-space pruning, based on a theory that unifies many existing methods. Their implementation reduced the number of decisions, but no speedup was obtained. In this paper, we generalize beyond supercubes, creating a theory we call *B-cubi* ...

Keywords: *SAT, formal verification, learning, search space pruning*

123 Effective formal verification using word-level reasoning, bit-level generality, and parallelism: Word level predicate abstraction and refinement for verifying RTL verilog
Himanshu Jain, Daniel Kroening, Natasha Sharygina, Edmund Clarke
June 2005 **Proceedings of the 42nd annual conference on Design automation**
Publisher: ACM Press
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Model checking techniques applied to large industrial circuits suffer from the state space explosion problem. A major technique to address this problem is abstraction. The most